

**REMARKS**

Claims 1-11 are pending in the present Application. Claims 1-4 and 11 are withdrawn from consideration.

1. A telephone interview was held with the Examiner on August 2, 2005 regarding independent claim 5.

Applicants respectfully thank the Examiner for holding an interview wherein the fact that present claim 5 specifically claims:

“supplying *the fluid electrode material* to the insulation layer, the fluid electrode material being allowed *to permeate the insulation layer*;  
*forming a gate electrode from the permeated fluid electrode material* to be in contact with the gate busline; “

was respectfully discussed. For example it was pointed out that in the present Figure 5, the insulation layer 8 is formed and then subsequently it receives a liquid or fluid electrode material *which permeates insulation layer 8.*

It was also discussed that this claimed fluid permeation process is very different from Dimitrakopoulos et al., US patent 6,335,539 in which a “self-assembled” “thiol monolayer 18” or “thiol compound” is formed *on top of the electrodes 16* as shown in Figure 1-3 for example.

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II. The anticipation rejection of claims 5-8 in view of Dimitrakopoulos et al., US patent 6,335,539.

The USPTO states in paragraph 5 of the Office Action that Dimitrakopoulos discloses the limitations of claim 5 in Figure 3.

Additionally, the USPTO cites the text at col. 6, lines 33-41. However, Col. 5, lines 39-47 of Dimitrakopoulos et al. reads: "The organic semiconducting material is a solvent sensitive material including, but not limited to: pentacene, ...has a thickness of from about 100 to 1000 Å." Herein, this passage does not disclose supplying the fluid electrode material to the insulation layer. Column 6, lines 33-41 of Dimitrakopoulos et al. reads as, "FIG. 1 (and above description) illustrates... Specifically, in FIG. 3, electrode 16 may be formed on substrate 10 and then patterned. Self-assembled monolayer 18 is then formed on the electrodes and next organic semiconductor 20 is deposited. After deposition of the organic semiconductor, gate insulator 12 is formed, and the gate 14." Herein, there is no description that the fluid electrode material is allowed to permeate the insulation layer so that a gate electrode is formed from the permeated fluid electrode material.

Further, the USPTO states, "...forming a gate electrode (20) from the permeated fluid electrode material to be in contact with the gate busline (the Examiner considers numerical number 14 as gate busline) (col. 6, lines 33-41;...". However, numerical number (20) shows an organic semiconductor, and further, the organic semiconductor does not contact the gate busline 14 (see Fig. 3).

Also, there is neither disclosure nor suggestion in Dimitrakopoulos et al. of the process as claimed comprising the steps of forming a gate insulating layer on the gate electrode; and after that, forming a semiconductor layer on the gate insulating layer. In

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column 6, lines 40-41 of Dimitrakopoulos et al. there is description, "After deposition of the organic semiconductor, gate insulator 12 is formed, and then gate 14." That is, the order of the gate insulating layer formation step and the semiconductor layer formation step in the invention is quite different from that in Dimitrakopoulos et al.

The dependent claims are therefore also allowable.

### III. Conclusion.

Reconsideration and allowance of all of the claims is respectfully requested.

If there are any additional charges with respect to this Amendment or otherwise, please charge them to Deposit Account No. 06-1130.

Please telephone the undersigned for any reason to expedite prosecution of the application.

Respectfully submitted,

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